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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/544,822	04/06/2000	Tongbi Jiang	4241US	9308

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/544,822	JIANG, TONGBI	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-64* is/are pending in the application.

4a) Of the above claim(s) *33-57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-32 and 58-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8-17-5 has been entered.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 58-62 and 64 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Yamada (5959363).

At column 56, line 12 to column 58, line 24, Yamada discloses the following:

A method for attaching a semiconductor assembly, said method comprising: providing a semiconductor device 201 having an active surface;

providing a substrate 202 having an upper surface; applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and applying a flowable underfill material 206 between the substrate and the semiconductor device, such that said flowable underfill material contacts said applied wetting agent layer 205 "coupling agent". 59. (Previously Presented) The method according to claim 58, wherein applying said wetting agent layer comprises a dispensing "screen printing" method 60 Presented) The method according to claim 58, wherein said wetting agent layer comprises at least one layer. 61. (Previously Presented) The method according to claim 58, wherein said wetting agent layer comprises a silane-based material.

A method for attaching a semiconductor assembly, said method comprising: providing a semiconductor device 201 having an active surface, a first end, a second end, a first lateral side end and a second lateral side end; providing a substrate 202 having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; applying a silane-based material layer 208 to one of a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate; connecting said semiconductor device to said substrate so

that said active surface of said semiconductor device faces said upper surface of said substrate; and applying a flowable underfill material 206 between said semiconductor device and said substrate, such that said flowable underfill material contacts said applied silane-based material layer.

A method for applying a material between a semiconductor device having a surface and a substrate having a surface, said semiconductor device mounted on said substrate, said method comprising: applying a essentially uniform liquid (inherent in "screen printing") silane-based wetting agent layer 205 inherently having a thickness of about a monolayer to at least one of said surface of said semiconductor device and said surface of said substrate; and applying a flowable underfill material between the substrate and the semiconductor device separately from said liquid silane-based wetting agent layer, such that said flowable material contacts said wetting agent layer.

To further clarify the disclosure of layer 205 inherently having a thickness of about a monolayer, the scope of the language "a thickness" is not limited to the total thickness. In addition, Yamada discloses the layer inherently having a thickness of about a monolayer because the layer inherently is at least a monolayer thick, and, when the total thickness of the layer is greater than a monolayer, the layer inherently has a thickness of about a monolayer at least intermediate the total thickness of the layer.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (5959363).

Yamada is applied as applied supra.

However, Yamada does not appear to explicitly disclose the particular claimed layer thickness.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular thickness because applicant has not disclosed that, in view of the applied prior art, this layer dimension is for any additional purpose, and it appears prima facie that the process would possess utility using another thickness. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725

F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada as applied to claim 64 supra, and further in combination with Hieda (6303277).

Yamada does not appear to disclose literally the layer 205 having a thickness of about a monolayer.

Nonetheless, at column 3, line 64 to column 4, line 5; and column 5, lines 41-51, Hieda discloses literally a layer 2 having a thickness of about a monolayer. Furthermore, it would have been obvious to combine this disclosure of Hieda with the disclosure of Yamada because it would enable obtainment of a high resolution layer pattern.

Claims 1-5, 7-12, 15, 22 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yamada (5959363), Schultz (6350840) and Pluddemann (4961967).

At column 53, line 66 to column 56, line 11; and column 59, line 34 to column 60, line 53, Yamada discloses the following:

A method for applying a material between a semiconductor device having a surface and a substrate having a surface, said method comprising: applying a liquid "alcoholate" wetting agent layer 208) to one of said surface of said semiconductor device and said surface of said substrate; and

applying a flowable underfill material between the substrate and the semiconductor device, such that said flowable material contacts said wetting agent layer; wherein said semiconductor device is attached to said substrate; wherein said applying said liquid wetting agent layer comprises a dispensing method "coated on the surfaces of the semiconductor chip and the wiring circuit board"; wherein said liquid wetting agent layer comprises at least one layer; wherein said liquid wetting agent layer comprises a plurality of layers 207, 208; wherein said applying a liquid wetting agent layer comprises providing a material that to the surface of one of said surface of said semiconductor device and said surface of said substrate for the application of an underfill material.

A method for applying a material between a semiconductor device and a substrate, said method comprising: providing a semiconductor device having an active surface, another surface, a first end, a second end, a first lateral side, and a second lateral side, said first end, said second end, said first lateral side, and said second lateral side forming at least a portion of a periphery of said semiconductor device; providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; applying a liquid wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; and applying a flowable underfill material between said

semiconductor device and said substrate, such that said flowable material contacts said applied wetting agent layer; wherein said flowable material is applied substantially adjacent to at least one end of said semiconductor device; wherein said flowable material substantially fills a gap between said semiconductor device and said substrate; wherein said flowable material is provided substantially adjacent to said at least a portion of the periphery of said semiconductor device to fill a gap between said substrate and said semiconductor device; wherein said applying said flowable material comprises: providing said flowable material substantially adjacent said first end of said semiconductor device for filling between said substrate and said semiconductor device by one or more forces acting upon said flowable material.

However, Yamada does not appear to explicitly disclose that the underflow material is a thermoplastic material.

Nevertheless, as cited, Yamada discloses that the underflow material is a thermosetting material. Moreover, at column 70, lines 8-14 and 62, Yamada discloses that the underfill material is not limited to thermosetting material. In addition, at column 1, line 32 to column 4, line 63, Schultz discloses a thermoplastic underfill material. Hence, it would have been obvious to combine this disclosure of Schultz with the disclosure of Yamada

because it would provide a reworkable underfill that is superior to the thermosetting underfill of Yamada.

Also, Yamada and Schultz do not appear to explicitly disclose that said flowable material contacts said liquid wetting agent layer; wherein said liquid wetting agent layer includes a layer of silane-based material; wherein said liquid wetting agent layer comprises one of glycidoxypropyltrimethoxysilane and ethyltrimethoxysilane.

Regardless, as cited, Yamada discloses that "other adhesion assistants [wetting agent layers] may also be coated." Also, at column 1, third full paragraph, (in Plueddemann, at column 1, lines 5-8, 21-23 and 55-63; column 2, lines 5-49; column 3, lines 22-54; column 3, line 65 to column 4, line 10; column 4, lines 24-27 and 58-62; column 6, lines 11-19, 37-44 and 57-65; and column 7, line 4 to column 8, line 5, incorporated by reference), Pluddemann discloses that a flowable material contacts a liquid wetting agent layer; wherein the liquid wetting agent layer includes a layer of silane-based material; wherein the liquid wetting agent layer comprises one of glycidoxypropyltrimethoxysilane and ethyltrimethoxysilane. In addition, it would have been obvious to combine this disclosure of Pluddemann with the disclosure of Yamada and Schultz because it would provide the "other adhesion assistants" of Yamada having improved wetting to the thermoplastic underfill material of Yamada and Schultz.

Claims 13, 14, 16-21 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, Schultz and Pluddemann as applied to claim 10, and further in combination with Akram (5766982).

Yamada, Schultz and Pluddemann do not appear to explicitly disclose the following:

The method wherein said substrate includes an aperture extending through said substrate; wherein said aperture is located adjacent to said another surface of said semiconductor device, further comprising: elevating at least said first side wall of said substrate and said first end of said semiconductor device; wherein said elevating said first side wall of said substrate comprises placing said substrate on a support structure and elevating at least one portion of said support structure, further comprising: providing a dam on the substrate adjacent to at least one of said first end, said second end, said first lateral side and said second lateral side of said semiconductor device; wherein said dam extends to substantially between said semiconductor device and said substrate, further comprising: vibrating one of said semiconductor device and said substrate; wherein said vibrating one of said semiconductor device and said substrate comprises placing said substrate on a support structure and vibrating said support structure; wherein said substrate includes at least one aperture extending through said substrate and substantially located adjacent to said another surface of said

semiconductor device; wherein said flowable material is provided through said at least one aperture of said substrate substantially filling a gap between said substrate and said semiconductor device; wherein said substrate includes at least one aperture extending therethrough and substantially located adjacent to said another surface of said semiconductor device; wherein said flowable material is provided from below said substrate; and wherein said flowable material is provided through said at least one aperture contacting at least a portion of said another surface of said semiconductor device.

Nevertheless, at column 4, line 36 to column 7, line 17, Akram discloses a process wherein a substrate 10 includes an aperture extending through a substrate, an aperture 60 is located adjacent (nearby) to another surface of a semiconductor device 12; elevating at least a first side wall of the substrate and a first end of the semiconductor device; wherein elevating a first side wall of the substrate comprises placing the substrate on a support structure 44 and elevating at least one portion of a support structure; providing a dam 40 on the substrate adjacent to at least one of a first end, a second end, a first lateral side and a second lateral side of a semiconductor device; wherein a dam extends to substantially between a semiconductor device and a substrate; vibrating 48 one of a semiconductor device and a substrate; wherein vibrating one of a semiconductor device and

a substrate comprises placing a substrate on a support structure and vibrating a support structure; wherein a flowable material 28 is provided through at least one aperture of a substrate substantially filling a gap 26 between a substrate and a semiconductor device; wherein the flowable material is provided from below the substrate; and wherein a flowable material is provided through at least one aperture contacting (at least indirectly physically and thermally contacting) at least a portion of another surface of a semiconductor device. Moreover, it would have been obvious to combine this disclosure of Akram with the disclosure of the applied prior art because it would facilitate applying the flowable material 206 between the substrate and the semiconductor device.

Also, in the combination, Yamada discloses the following:

The method wherein applying a flowable material comprises: providing the flowable material substantially adjacent to the first end of the semiconductor device for filling the gap between the substrate and the semiconductor device; wherein said applying said flowable material comprises: providing said flowable material substantially adjacent to said first end and one of said first lateral side and said second lateral side of said semiconductor device for filling the gap between said substrate and said semiconductor device.

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, Pluddemann and Shultz, as applied to claim 10, and further in combination with Banerji (5203076).

Yamada, Pluddemann and Shultz do not appear to explicitly disclose wherein said applying said flowable material between said semiconductor device and said substrate further comprises placing said semiconductor device and said substrate in a chamber, said chamber having an atmosphere therein having a variable pressure, further comprising: varying the pressure of said atmosphere in said chamber for said flowable material substantially filling a gap between said semiconductor device and said substrate.

Regardless, at column 2, lines 55-68; and column 3, lines 1-10, Banerji discloses wherein applying a flowable material 22 between a semiconductor device 10 and a substrate 20 comprises placing the semiconductor device and the substrate in a chamber 32 having an atmosphere therein having a variable pressure, and varying the pressure of the atmosphere in the chamber for the flowable material substantially filling a gap 18 between the semiconductor device and the substrate. Furthermore, it would have been obvious to combine this disclosure of Banerji with the disclosure Yamada, Pluddemann and Shultz because it would facilitate applying the flowable material 206 between the substrate and the semiconductor device.

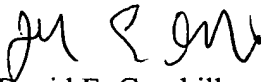
Applicant's amendment and remarks filed 8-17-5 have been fully considered and are adequately addressed by the rejections supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR:
Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.



David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
18-Nov-05